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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/600,959
Filing Date: June 20, 2003
Appellant(s): MALIK ET AL.

Robert L. King (#30,185)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 28 June 2005.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of invention contained in the brief is correct.

(6) Grounds of Rejection to be reviewed on Appeal

The appellants' statement of the grounds of rejection is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,636,927	Peters et al	10-2003
6,085,291	Hicks et al	07-2000

(9) Grounds of Rejection

From previous Office action:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-10, 13-16, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Peters et al (US Patent 6,636,927).

With respect to independent claim 1, a method for configuring a prefetch buffer, comprising receiving a read request from a master, and, in response to the read request, selectively modifying a "total length of one (or more) prefetch buffer lines" (data size) of the prefetch buffer based on an attribute of the read request to an adjusted line size, the prefetch buffer having lines of differing total length during operation is disclosed in the abstract in the last ten lines, specifically. The "total length of one buffer line" is the same as the "data size" of Peters et al. "...that eliminates dedicating unused buffer storage to the replacement entry of the prefetch buffer" is an "intended use" limitation which the system of Peters et al inherently anticipates, as the explicitly anticipated apparatus is clearly able to eliminate dedicating unused buffer storage to the replacement entry of the prefetch buffer. While features of an apparatus may be recited

either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. MPEP 2114.

With respect to claim 2, the attribute of the read request comprising a master identifier corresponding to the master is disclosed in the abstract as a prefetch control register being associated with the a master device, the prefetch control register being associated with a particular master device inherently identifies the master.

With respect to claim 3, selectively modifying the total length of one or more prefetch buffer lines being "based on" a second attribute of the read request, wherein the second attribute comprises a data size is disclosed in the abstract as the prefetch size.

With respect to claim 4, the read request resulting in a miss in the prefetch buffer is disclosed in column 4, lines 38-40. When the prefetch buffer does not have the data, the data is not transferred from it, which is, by definition, a miss.

With respect to claim 5, the prefetch buffer including a plurality of lines, each of the lines having a "corresponding one" of "status fields," is disclosed in column 3, lines 50-57. The prefetch control registers "correspond" to the buffers that have lines.

With respect to claim 6, selecting at least a portion of the plurality of lines as a "replacement entry" within the prefetch buffer based on the status fields of the prefetch buffer is disclosed in column 4, lines 41-47.

With respect to claim 8, selectively modifying the total length of one or more prefetch buffer lines comprising selectively modifying a line size of the replacement entry is disclosed in column 4, lines 41-47. If the buffer has different segments, each

assigned to different masters, and, as discussed supra, each master has it's own respective line size, then the line size of the "replacement entry" will be different than the original.

With respect to claims 9 and 16, selectively modifying the line size of the replacement entry comprising selectively modifying a status field corresponding to the replacement entry is disclosed in column 7, lines 29-31 as the register is programmable.

With respect to claim 10, selectively modifying the status field corresponding to the replacement entry being based on the attribute of the read request, the attribute comprising a data size is disclosed in column 8, line 42, for example, as the prefetch size.

With respect to claim 13, generating at least one data request to a memory addressed by the read request and storing data from the memory into the replacement entry of the prefetch buffer is disclosed in column 3, lines 50-57. Examiner notes that claim 13 merely describes how a buffer works, by definition.

With respect to independent claim 14, a method for configuring a prefetch buffer is disclosed in the abstract.

Receiving a read request to a memory from a requesting master, the read request having a "corresponding " data size (prefetch size) and burst length (bursting is disclosed in column 2, line 33 and inherently has a length as discussed supra, is disclosed in column 3, lines 37-42 and 50-57.

Providing a prefetch buffer reconfiguration indicator "based on" the data size and the burst length is disclosed in column 3, lines 37-42.

Selecting a replacement entry within the prefetch buffer and based on the prefetch buffer reconfiguration indicator, selectively modifying total length of the replacement entry of the prefetch buffer based on an attribute of the read request to an adjusted line size and storing the data fetched from the memory in the replacement entry is disclosed in column 4, lines 41-47. Inherently, buffers are filled and emptied as needed – otherwise, once they filled, they would no longer be useful if the data in them is no longer needed by the master. Accordingly, the registers are programmable for future prefetches. "...that eliminates dedicating unused buffer storage to the replacement entry of the prefetch buffer" is an "intended use" limitation which the system of Peters et al inherently anticipates, as the explicitly anticipated apparatus is clearly able to eliminate dedicating unused buffer storage to the replacement entry of the prefetch buffer. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. MPEP 2114.

With respect to claim 15, the prefetch buffer reconfiguration indicator being "based on" the data size (prefetch size), the burst length (discussed supra), and a master identifier corresponding to the requesting master (also discussed supra) is disclosed in column 3, lines 37-42 as the prefetch control register.

With respect to claim 19, generating at least one data fetch request to the memory wherein the at least one data fetch request is "based on" a bus width corresponding to a memory is disclosed in figure 5, #506. Data fetches are inherently

"based on" a bus width in that only s much data can be fetched at a time, depending on the size (width) of the bus carrying it.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters et al (cited supra) in view of Hicks et al (US Patent #6,085,291).

With respect to claims 17 and 18, Peters et al disclose the limitations of the claims upon which the instant claims depend. Peters et al disclose a status field in the prefetch registers.

The difference between Peters et al and the instant claims, however, are the explicit recitations of the status field comprising an address tag field, wherein selectively modifying the at least one status field comprises selectively modifying the address tag field as well as selecting the replacement entry within the prefetch buffer comprising checking a valid bit within the status field of the prefetch buffer.

However, Hicks et al disclose the address tag field and modification of same in figure 3, "ADR" as well as in figure 5, "LINE ADR." In addition, figure 5 shows the valid bit being a part of the stream address buffer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Peters et al and Hicks et al before him/her,

to utilize the address tag field and valid bits of Hicks et al in the status field of Peters et al, because the address bit can be used to allocate the corresponding data into the buffer, as discussed by Hicks et al in column 6, lines 43-45, for example, as well as use of the valid bit in the status being used to indicate whether the stream (data) is allocated, as discussed by Hicks et al in column 6, line 50, for example.

Allowable Subject Matter

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 20-22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 7 and 20, the claimed combination of fields is not taught or suggested by the cited prior art of record, nor is there any motivation to combine the fields that are actually disclosed, such as the valid field and address tag, as discussed supra, with the additionally claimed fields of the instant claims, such as, e.g., the "used" field. Claims 21-22 depend upon claim 20 and are allowable for at least the reasons set forth supra with respect to same.

Response to Arguments

With respect to applicants' arguments regarding the length of the buffers of the instantly claimed invention being variable, while the buffer length of Peters et al are fixed. Examiner notes, however, that this is not commensurate in scope with the instant

claim limitations – applicants recite, in the instant independent claims, "modifying total length of one or more prefetch buffer lines." In order to anticipate this limitation, the prior art need only show one buffer line at a time of different sizes, not different sizing of entire buffers, as applicants argue instantly.

However, even if applicants did claim such features, examiner refers applicants to figure 5, which discloses a "specified prefetch size" in an associated control register.

With respect to applicants' argument that because the recited invention dynamically varies the total length or line size to optimize buffer storage, the Peters et al reference does not anticipate the claimed invention. Examiner again notes that this argument is not commensurate with the claim language – "selectively" may be different from "dynamically," for example. However, examiner maintains that Peters et al indeed anticipates the claim language. The examiner has equated the "data size" of Peters et al to the "line size," or "total length of one prefetch buffer line," as is instantly claimed.

With respect to applicants' argument that Hicks et al do not teach or suggest "selecting the replacement entry within the prefetch buffer comprising checking at least one of a valid, invalid, or used bits within status fields of the prefetch buffer," or using an address tag field as a status field, examiner respectfully disagrees. It is also important to note that applicants have not clarified whether the address tag field and the tag field are the same field, as was requested in the previous Office action. The instant amendment to the specification does not clarify the question at all, nor do applicants attempt to clarify the point in their response. While the metes and bounds of the claim may be determined to satisfy 35 USC 112, 2nd paragraph, if the fields are not the same,

there may be enablement and written description issues under 35 USC 112, 1st paragraph.

(10) Response to Argument

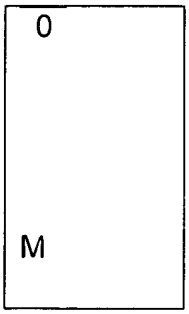
Before addressing applicants' specific arguments, examiner wishes to further clarify his position and characterize applicants' arguments in general terms to facilitate a clear understanding of the instant issues.

In general, it appears the issues at hand boil down to claim interpretation. It appears applicants' position is that examiner has taken an unreasonably broad interpretation of the claim language. Examiner believes applicants have taken too narrow an interpretation of same.

The "total length of one or more prefetch buffer lines" may be interpreted in two ways:

1. "total length of one prefetch buffer line" (0...N)

2. "total length of more than one prefetch line" (0...M)



In the previous Office action, examiner had taken the first interpretation. However, both interpretations are anticipated by Peters et al (cited and applied in previous Office actions), as will be discussed in significantly more detail below.

Using claim 1 as representative, for example, a method for configuring a prefetch buffer is disclosed in column 7, lines 26-31.

Receiving a read request from a master is disclosed in column 4, line 43, e.g.

In response to a read request (column 9, line 4), selectively modifying [the prefetch buffer] is disclosed by Peters et al in column 9, lines 25-31, which discusses setting the fields of a control register according to the parameters of the read command from a particular master. Column 7, lines 25-28 discuss that each prefetch control register is associated with one master. Thus, prefetch sizes that are optimized (modified) for associated master can be stored in the control register to optimize performance.

The "total length of one or more prefetch buffer lines," is broad, as discussed supra. It may be interpreted as the cache line size (buffer width) or the total number of cache lines (buffer depth). Either way, the fields of each of the control registers of Peters et al are set according to both dimensions. Field F0 sets the prefetch size with respect to the adjusted line size or cache line size (buffer width), as discussed in column 9, lines 32-34. Field F2 sets the number of cache lines to be prefetched (buffer depth), as discussed in column 9, lines 34-44. Accordingly, both the width and depth of the buffer to be dedicated are set via the fields in the control register, "based on an

attribute of the read request," which is the master ID in the read request that selects the appropriate control register.

This inherently results in elimination of dedication of buffer storage to unused portions of the one or more prefetch buffer lines. The instant specification does not provide a more specific discussion of what "unused portions" of a dedicated buffer are, so examiner has used the ordinary meaning of "unused portions" of a dedicated buffer, which are portions within the dedicated buffer that would not actually be filled with data. By dedicating buffer space for only what is needed for that particular read command, there is inherently no "unused space" in the dedicated buffer.

"The prefetch buffer having lines of differing total length during operation," does not specify whether the dedicated buffer of multiple lines has each line being different size for that read command. "During operation" does not specify how many read commands should be considered an "operation." Accordingly, as the cache line size is set to different respective sizes for three consecutive read commands, for example, the buffer in general has lines of differing total length (assuming this means cache line size, and not the total number of lines, in this case) during operation (which is the operation of three consecutive read commands).

It is with the above interpretations in mind that the arguments with respect to each specific claim are addressed below.

Independent Claim 1

With respect to appellants' argument in the third paragraph of page 6 of the instant brief, that the method of claim 1 avoids the necessity of having various fixed-size

prefetch buffers, each of differing size, to efficiently interface with multiple bus masters, examiner respectfully disagrees. This argument is not commensurate with the claim language.

Appellants continue from the bottom of page 6 of the instant brief into page 7 to compare the figures of the instant disclosure to the figures of the applied prior art. Examiner notes that such a comparison is irrelevant to the claim language, and also notes that figure 7 of the applied prior art is merely exemplary of one particular embodiment of the disclosure (see column 9, e.g.), and was not relied upon to reject the instant claims during prosecution. However, examiner wishes to note that column 10, lines 6-9 discuss the fact that the segments of figure 7 may, indeed, be programmed to provide additional flexibility. Appellants also recite that, "within the method of claim 1 multiple bus masters may efficiently use a same portion of the prefetch buffer." However, no such limitation is present in the claim. In fact, no such limitation appears to be in the instant specification, either. Accordingly, appellants' arguments are not commensurate in scope with the claim language.

Dependent Claims 2-6, 8-10 and 13

With respect to claim 2, appellants characterize the attribute of the read request as *being* one of three attributes including a master identifier corresponding to the master. However, the claim language does not use the word "being," instead using the word "comprising." This is important, as "being" precludes other options, whereas "comprising" leave open the possibility of other options in addition to those claimed. Appellants continue by noting that in the Peters et al system, clearly, there is

information which identifies which master requests an action. Examiner agrees. However, appellants continue by reciting that claim 2 recites using a master's identity to selectively modify a prefetch buffer line length when the master generates a read request. While examiner agrees that this option is, indeed, within the scope of the claim language, so are others, as discussed supra. The claim language does not limit it to just this option. However, as also discussed supra, the Peters et al reference actually anticipates this option anyway. Appellants go on to recite that claim 2 also recites using a data size of the read request and a burst length of a read request to selectively modify a prefetch buffer line length. However, the actual claim language uses the phrase "one of." This means in the alternative. Accordingly, the applied prior art need only discuss any one of the options claimed, which it does, as discussed supra. Therefore, appellants' arguments are not commensurate in scope with the claim language.

With respect to claim 3, appellants argue that Peters et al do not teach or suggest the combination of claims 1, 2, and 3, as recited in claim 3, examiner respectfully disagrees, as discussed with respect to the limitations of claims 1 and 2 as discussed supra. Column 9, lines 30-31 discusses fields used in the control registers for prefetching from a source device, for various data transfer commands. It is also very important to note that "data size," as recited in the instant claim, is defined in the instant specification at page 7, lines 2-4, which recite, "the data size signal determines the size of a single unit of data within each burst line." Lines 6-7 continue, "other data sizes such as multiple words or a byte could be indicated by the data size signal."

Accordingly, data size may mean data of any size, as the sizes given are merely exemplary, and do not limit the term.

With respect to claim 4, appellants argue that claim 4 recites that a prefetch buffer line size is selectively modified when there is a miss in the buffer, and that Peters et al do not teach the recitals of claims 4 and 1 at column 4, lines 38-40. However, claim 4 merely recites, "wherein the read request results in a miss in the prefetch buffer." Column 4, lines 38-40 disclose that when the prefetch buffer contains the data, it is transferred. This is a "hit." The only other alternative is if the prefetch buffer does not contain the data. This is a "miss." The result has to be a hit or a miss – there are no other options possible. The data is either there or it isn't. The reference specifically discloses that when it is, it is transferred. However, inherently, if it isn't (a miss), then it can't be. The reference explicitly discloses the decision being made of whether or not the data is present, and, therefore, discloses a miss. Accordingly, appellants' argument is not commensurate in scope with the claim language.

With respect to claim 5, appellants argue that Peters et al do not disclose a prefetch buffer having lines with a status field. Again, appellants' arguments are not commensurate with the claim language. The claim requires "corresponding to," not "stored in." See the previous rejection supra.

With respect to claim 6, the arguments appear to be the same as in claim 5. Accordingly, examiner refers appellants to the discussion of same supra.

With respect to claim 8, appellants argue that Peters et al do not disclose a prefetch buffer with a status field in the buffer lines. As discussed with respect to claims

5 and 6, this is not commensurate with the claim language. Appellants continue to argue that Peters et al do not disclose the "selective modification" of buffer line length in response to a read request and clearly do not teach modification of the line size of a replacement entry. Examiner respectfully disagrees, and refers appellants to the rejection supra. In addition, appellants are referred to column 9, lines 32-55, e.g., which discloses that a tap point is set in the control register, so that while a dedicated buffer is emptying at one end, it can begin being filled at another, thus replacing entries that are "invalid," or emptied.

With respect to claims 9, 10, and 13, appellants argue that the claims recite further features not taught by Peters et al such as the modification of the status field in a prefetch buffer line. Examiner respectfully disagrees, and notes also that this requirement is not commensurate in scope with the claim language, as discussed supra with respect to claim 5, e.g.

Independent claim 14

With respect to independent claim 14, appellants argue that Peters et al do not teach "receiving a read request to a memory from a requesting master, the read request having a corresponding data size and burst length." Examiner respectfully disagrees, and refers appellants to the rejection of the instant claim supra. Burst length information is inherent in bursting, by definition – in order to burst information, the system MUST know how much information to burst. Appellants continue by arguing that Peters et al do not teach or suggest, "providing a prefetch buffer configuration indicator based on the data size and the burst length." Examiner respectfully disagrees. If using the

interpretation of "data size" to be any size of data, including multiple lines, then it is the same as the burst length. However, even if that interpretation is not taken, and "data size" is interpreted to be the same as the "cache line size," Peters et al still teach just such control in column 9, lines 32-55, e.g., which teaches that the F0 field would store a "data size," and the F2 filed would store a "burst length." A burst, by definition, is merely a transfer of a block of data without a break. That block may be any size. Appellants are also referred to the Answer herein with respect to claim 1. See the discussion supra in response to appellants' arguments regarding claim 8 for the tap point being indicative of "replacement entries." Examiner's responses to claim 1 arguments apply equally instantly.

Dependent claims 15, 16, and 19

With respect to claim 15, appellants argue that there is no teaching in the cited section of Peters et al of a "prefetch buffer reconfiguration indicator." Examiner refers appellants to the rejection supra. In addition, appellants are encouraged to review column 9, lines 32-55, which elaborates on the contents of the prefetch control register.

With respect to claim 16, appellants again appear to be confusing "corresponding to" with "in." See relevant discussion supra.

With respect to claim 19, Appellants argue that Peters et al do not teach a data fetch request being "based on" a bus width "corresponding to" the memory. Examiner respectfully disagrees as clearly noted in the rejection supra. Prefetching inherently is "based on" the width of the bus – more data than can fit in the bus cannot be fetched at a time. Accordingly, the fetching of data has to be "based on" the bus width in some

manner. For example, wasting bus bandwidth is discussed in column 2, lines 60-61 as a downfall of the prior art to Peters et al.

With respect to appellants' arguments that their position was "dismissed" in the previous office action, examiner regrets appellants interpreted his position as such. Examiner hopes that appellants do not feel examiner did not carefully and respectfully consider each and every argument put forth throughout prosecution. Examiner is, and has been, merely trying to articulate that appellants' arguments have not been commensurate in scope with the claim language. As discussed throughout the instant Answer, the effective sizes of the prefetch buffers in the bridge circuitry is disclosed by Peters et al as changing with the prefetch sizes loaded into the control registers respective to the masters. The size remains constant for each particular transfer in accordance with the fields of the control register and tap points, as discussed in column 9, lines 10-20 and 32-55, e.g., as discussed supra. This is what the claim language, as it stands instantly, requires.

Dependent claims 17 and 18

With respect to appellants' arguments regarding claims 17 and 18, examiner respectfully disagrees, and notes that appellants' arguments with respect to same appear to be dependent upon the rejections of the claims upon which they depend. The recited combination of features of claim 18 and claim 14 are, indeed, taught by the combination of Peters et al and Hicks et al, as discussed supra in the body of the rejection as repeated herein.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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August 27, 2005

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